UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,242	02/06/2004	Chang-Ho Cho	2557-000190/US	6461

30593 7590 04/19/2007

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
DAVIS, ROBERT B	
ART UNIT	**PAPER NUMBER**
1722	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,242	CHO, CHANG-HO	
	Examiner	Art Unit	
	Robert B. Davis	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-16* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suetaki (5,594,274: figures 2, 5, 6; column 1, lines 62-67; column 4, line 64 to column 5, line 5; and column 6, lines 32-67) taken together with Matsuura (JP 04-249121 A: figures 1 and 2 and the English abstracts) and Matsuda et al (4,812,420: figures 1-6 and column 2, lines 50-65).

Suetaki discloses opposed cavity blocks (20, 30) having a concave surface (25, 35) defining a cavity in which a semiconductor chip (2) is positioned, a gate (21) defining the resin entry of the resin into the cavity, wherein the gate is positioned in the corner of the mold cavity (figure 5 and column 4, line 64 to column 5, line 5) such that the resin flows in the mold cavity as shown in figure 5. It is clear from figure 5, that the resin flow hits the chip at an angle of around 45 degrees with respect to the two sides of the chip adjacent to the gate. In regards to claim 5, the reference illustrates a straight gate in the corner. The reference does not disclose a gate block, which is opened and closed, or a rectangular chip. The examiner is construing the chip as a positive element of the claim as amended and argued by applicant.

Matsuura discloses a molding cavity (1) for packaging a semiconductor element wherein a gate is defined to introduce resin into the molding cavity. The mold further includes a movable gate block (5), which closes the molding cavity after injection for the purpose of separating the cured runner from the cured article such that post mold deflashing of the runner is at least reduced if not eliminated.

Matsuda et al disclose a packaged semiconductor device having a rectangular chip (6).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Suetaki by providing a closable gate block within a mold as disclosed by Matsuura for the purpose of reducing post mold deflashing of the runner. The inclusion of the movable gate block reduces the amount of equipment required by the molding process in that post mold deflashing equipment can be reduced or eliminated. It would have been further obvious to modify the apparatus of Suetaki by using a rectangular chip as disclosed by Matsuda et al dependent upon the desired chip to be packaged. Suetaki discloses what appears to be a square chip and hence it would have been obvious to slightly modify the shape of the chip to a rectangular chip as disclosed by Matsuda et al.

Note that a translation of the Japanese reference is being ordered.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suetaki taken together with Matsuura and Matsuda et al as applied to claims 1-5 above, and further in view of Shin et al (6,717,248: figures 12B and 13, and column 12, lines 45-67).

The previous combination discloses all claimed features except for the use of a L-gate having two surfaces parallel with two sides of the chip.

Shin et al disclose an apparatus for packaging a semiconductor chip (2) having a gate (G) having a L-shaped gate (H) as illustrated in figure 12B.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Suetaki by having a L-shaped gate for the purpose of matching the gate shape to the edge of the chip.

4. Claims 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suetaki taken together with Matsuura and Matsuda et al and further in view of Shibata (6,717,248: figures 12B and 13 and column 12, lines 45-67) and Inoue (JP 11-176855).

The previous combination discloses all claimed features except for the die having a channel block. The Inoue reference discloses a plurality of pots (6) for storing and injecting resin with a ram.

Shibata disclose a mold die for packaging/encapsulating a semiconductor chip comprising: upper and lower cavity blocks (5D, 5C), a gate block (6C) and a runner or channel block (59) for distributing resin from a central source to a plurality of molding cavities.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Suetaki by providing a cavity block to supply a plurality of molding cavities with resin from a common source as disclosed by Shibata because such a separate channel block allows for replacement of individual parts

without replacing the entire mold die. It is further obvious to modify the apparatus of Suetaki by using a plurality of pots and rams for the purpose of feeding resin to a molding cavity. It is further obvious to use a channel system for supplying a plurality of mold cavities with resin from a central source as disclosed by Shibata because such a configuration reduces the amount of pots and plungers and thus reduces the amount of resin tablets supplied per molding operation by reduction of the number of pots.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suetaki taken together with Matsuura, Matsuda et al, Shibata and Inoue as applied to claim 10 above, and further in view of Park et al (6,642,610: figures 1a and 1b).

The previous combination discloses all claimed features except for the assembly including a pair of stacked chips connected by bonding wires.

Park et al disclose an assembly for encapsulating a plurality of semiconductor chips (2 and 4) connected by bonding wires (8a).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Suetaki by providing a pair of stacked chips connected by bonding wires as disclosed by Park et al as such was a well known packaged element as shown in figure 1a. It would have been obvious to use the previous combination with a well known stacked chip assembly dependent upon the chip architecture of the desired product of the mold.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suetaki taken together with Matsuura and Matsuda et al as applied to claims 14 and 15 above, and further in view of Bigler et al (5,517,056: figure 4).

The previous combination discloses all claimed features except for the presence of low bonding wire density at the corner of the gate and vents.

Bigler et al disclose a chip assembly having leads (35) absent in the gate portion (44) and the opposing diagonal portion (42).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the method of Suetaki by using a chip assembly having no leads adjacent the gate and the opposing diagonal as disclosed by Bigler et al such that the leads are not disrupted by the gate and venting portions of the cavity.

Allowable Subject Matter

7. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-7 and 10-16 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Davis whose telephone number is 571-272-1129. The examiner can normally be reached on Monday-Friday 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert B. Davis
Primary Examiner
Art Unit 1722

4/16/07